(12) UK Patent Application (19) GB (11) 2 267 291 (13) A

(21) Application No 9211242.4

(22) Date of filing 27.05.1992

(71) Applicant
Northern Telecom Limited

(Incorporated in Canada - Quebec)

World Trade Center of Montreal, 380 St Antoine Street West, Montreal, Quebec, Canada

(72) Inventors
Rudolf August Herbert Heinecke
Peter Gordon Eldridge

(74) Agent and/or Address for Service
J P W Ryan
Northern Telecom Europe Limited, Patents and Licensing, West Road, Harlow, Essex, CM20 2SH, United Kingdom

(51) INT CL⁵
C23C 16/30 16/40, H01L 21/70

(52) UK CL (Edition L)
C7F FCXX FHE FR841 FR913 FR919 F103 F303 F306 F809
H1K KJAC K1FD K5B1 K5B2 K5C3G
U1S S2088 S2089

(56) Documents cited
GB 2175137 A	GB 1264163 A	GB 1153794 A
EP 0422243 A1	WO 90/15018 A1	WO 88/04333 A1
US 5037514 A	US 4634635 A	US 4572841 A
US 4410559 A		

(58) Field of search
UK CL (Edition K) B6J JME JMF JMY, C7F FHB FHE FHZ, H1K KJAC
INT CL⁵ C23C, H01L
Online databases: WPI, CLAIMS

(54) Integrated circuits; depositing silicon compounds using excess hydrogen

(57) A planarised insulating film of a refractory silicon compound such as silica or a silica boxed glass is provided on a non-planar integrated circuit structure, e.g. an opto-electronic circuit, by deposition from a plasma containing the precursor of the silicon compound, e.g. a silane, an oxidising agent and an excess of hydrogen. The film may subsequently be etched to provide windows and providing electrical contact to the circuit via said windows. The plasma may further incorporate a hydrogen, e.g. methane. The oxidising agent may be nitrous oxide and the plasma may further incorporate a hydrocarbon such as methane.

GB 2 267 291 A

PLASMA DEPOSITION PROCESS

This invention relates to a plasma deposition process for fabricating non-planar integrated circuits, e.g. opto-electronic circuits.

One of the most difficult problems in the fabrication of non-planar e.g. opto-electronic integrated circuit devices is that of providing a planarising surface film through which contact windows are subsequently etched to access the circuit devices. This is a particular problem in the fabrication of opto-electronic circuits which differ from conventional (silicon) integrated circuits in two important respects. Firstly the nature of current opto-electronic devices requires a significant departure from planarity and, secondly, the device structure and materials employed are thermally sensitive thus precluding high temperature processing.

Attempts have been made to deposit surface films of refractory materials, such as silica, by a plasma process similar to that employed in the fabrication of conventional integrated circuits. However, it has been found that these techniques result in the well-documented problem of non-uniform coverage of steps and trenches. At the edge of such a discontinuity a thin band of very defective material is formed. The effect causes cusping resulting in negative surface slopes and voiding, and in reduced insulation thickness. When this insulator layer is subsequently etched to form contact windows it is found that significant loss of definition occurs in those regions of defective insulation. Specifically, the etching process results in deep crevicing in these defective regions, and the contact openings thus formed can then be very difficult to metallise effectively.

A number of process techniques have been developed in an attempt to address this problem. These techniques include the use of polyimide films, resist etch-back, single and double spin-on glass and multiple deposition-etch processes. All these techniques have one or several disadvantages including poor process control, electrical damage, multiple equipment and handling requirements and considerably extended process time. Alternatively, tetra-ethyl oxysilane (TEOS) is used as a precursor, giving improved planarisation, but requires complicated gas handling techniques and provides only a partial solution to the problem.

The object of the invention is to minimise or to overcome these disadvantages.

According to one aspect of the invention there is provided a process for depositing a substantially planar insulating film of a refractory silicon compound on an integrated circuit, the process including exposing the circuit to a plasma containing the precursors of the silicon compound together with excess hydrogen whereby to provide a uniform coating of the circuit.

According to another aspect of the invention there is provided a process for providing contacts to an integrated circuit, the process including exposing the circuit to a plasma containing a silicon compound, an oxidising agent and excess hydrogen whereby to provide a substantially planar silica film on the circuit, selectively etching said silica film to define contact windows, and providing electrical contact to the circuit via said windows.

We have found that the addition of excess hydrogen to the deposition gas mixture provides a very significant improvement in the quality of deposited material and in the planarity of the deposited film thus substantially eliminating the problem of crevicing during the subsequent window etching process. Advantageously the deposited material comprises silica or a silica based glass. The plasma may be a continuous plasma or a pulsed plasma.

Typically, the gas composition used to deposit a silica film comprises a mixture of silane, nitrous oxide and hydrogen. The silica may be provided in a nitrogen carrier and the gas may further

incorporate a hydrocarbon such as methane.

We have found that a particularly effective gas mixture comprises:-

2 % Silane in hydrogen	200 sccm
Nitrous oxide	710 sccm
Methane	100 sccm

The gas proportions being defined in standard cubic centimetres per minute. We have employed this gas mixture for the deposition of silica films at a pressure of 800 mtorr and a temperature of 350°C using a 50 watt 13.54 MHz generator. The equipment employed had a parallel plate electrode system with an energy density of about 40 mW/cm^2.

Silica films deposited from this gas mixture are substantially planarised and display good defect-free coverage of steps and trenches. As a result, when the films are etched e.g. to define contact windows, the formation of crevices during window etching over steps is substantially eliminated. Another important observation is the low etch rate of the deposited film in hydrogen fluoride solution, as this indicates a densification effect due to the enhanced surface mobility. This is quite contrary to the possibility that the films might contain more water than that of a film produced by a conventional process and is unexpected in view of the presence of both hydrogen and an oxidising agent in the gas mixture.

Typically the volume ratio of hydrogen to silane in the gas mixture is greater than 10:1.

For comparative purposes we have also plasma deposited silica films using the above gas mixture but with the omission of hydrogen. Such films have a poor coverage and exhibit severe crevicing over steps or trenching when etching of contact windows is attempted.

An important aspect of the process is that it can be readily implemented on existing process equipment by a change in the process software and using processing gases in common use. Its implementation greatly simplifies the processes currently in use for the fabrication of multilevel interconnects of VLSI circuits and is also applicable to the fabrication of high integrity optical wave guide structures.

It will be appreciated that the gas mixture and process conditions will be adapted to the particular application. In particular, the type and the abundance of the effective intermediate species will be a function of substrate temperature, plasma density and ion bombardment for any given hydrogen concentration. None of these is critical but there will be an optimum operating band for each parameter.

It is thought that the process derives from the formation of a pseudo-liquid intermediate precursor phase on the substrate surfaces. The optimum use of such a phase extends the scope of the process to that of full planarisation processing. The significance of this concept is that the vapour pressure of such a (high mobility) surface phase would be lowest at the foot of a step and highest at the top corner. As a result the abundance of the species involved would be highest at the bottom of steps and trenches, exactly where they are needed most for planarisation purposes.

There are applications where the addition of hydrogen under optimised operating conditions will suffice to achieve an optimum result. However, methane or other organic materials can be added as well so as to include the formation of organo-metallic intermediates.

The technique is further applicable to ion assisted and sputtering processes. For instance, planarised, large grained aluminium metallisations with enhanced electro migration resistance may be produced by sputtering in a gas mixture containing hydrogen and an organic gas, and using substrate temperatures up to $300^{\circ}C$.

Finally, the technique is equally applicable to planarising operations by ion assisted etching (plasma or RIE). Under optimised conditions the addition of large proportions of H_2 or H_2/CH_4 mixtures to the etching gas (e.g. CF_4 for oxides) protects selectively deep trenches and holes by the increased abundance of the pseudo-liquid phase in these locations, thus resulting in their effective removal while the film is plasma etched.

Whilst the conformal coating process has been described with particular reference to opto-electronic circuits, it may also be applied to other non-planar circuit structures such as bolometer devices and silicon integrated circuits.

CLAIMS:-

1.   A process for depositing a substantially planar insulating film of a refractory silicon compound on an integrated circuit, the process including exposing the circuit to a plasma coating the precursors of the silicon compound together with excess hydrogen whereby to provide a uniform coating of the circuit.

2.   A process for providing contacts to an integrated circuit, the process including exposing the circuit to a plasma containing a silicon compound, an oxidising agent and excess hydrogen whereby to provide a substantially planar silica film on the circuit, selectively etching said silica film to define contact windows, and providing electrical contact to the circuit via said windows.

3.   A process as claimed in claim 2, wherein the oxidising agent comprises nitrous oxide.

4.   A process as claimed in claims 2 or 3, wherein the plasma further incorporates a hydrocarbon.

5.   A process as claimed in claim 4 wherein the hydrocarbon is methane.

6.   A process as claimed in any one of claims 2 to 5, wherein the silicon compound is silane.

7.   A process as claimed in claim 6, wherein the volume ratio of hydrogen to silane in the plasma is at least 10:1.

8.   A process for providing contacts to an integrated circuit which process is substantially as described herein.

9.   An integrated circuit treated by a process as claimed in any one of claims 1 to 8.

Patents Act 1977
Examiner's report to the Comptroller under Se .ion 17 (The Search Report)

Application number	
9211242.4	

Relevant Technical fields

(i) UK Cl (Edition   K   )   C7F (FHB, FHE, FHZ); B6J (JME, JMF, JMY); H1K (KJAC)

(ii) Int CL (Edition   5   )   C23C; H01L

Databases (see over)

(i) UK Patent Office

(ii)   ONLINE DATABASES: WPI, CLAIMS

Search Examiner

P G BEDDOE

Date of Search

14 JULY 1992

Documents considered relevant following a search in respect of claims   1 AND IN PART 9

Category (see over)	Identity of document and relevant passages		Relevant to claim(s)
X,A	GB 2175137 A	(MOBIL SOLAR) see especially Claim 1; Example 1	1, 9
X,A	GB 1264163 A	(WESTERN ELECTRIC) see especially page 2 line 17-35	1, 9
X,A	GB 1153794 A	(IBM) see especially page 2 lines 31-44	1, 9
X,A	EP 0422243 A1	(CANON) see especially Claim 1 Example 4; Table 5	1, 9
X,A	WO 90/15018 A1	(SUMITOMO) see Example 1	1, 9
X,A	WO 88/04333 A1	(BP) see especially Claim 1; Example 1	1, 9
X,A	US 5037514 A	(SEMICONDUCTOR) see especially excerpts 3, 4	1, 9
X,A	US 4634635 A	(KABUSHIKI) see especially Claim 3; Table	1, 9
X,A	US 4572841 A	(RCA) see especially Claim 1; Example 1	1, 9
X,A	US 4410559 A	(HAMAKAWA) see especially Figure 1; column 3 lines 31-57	1, 9

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family, corresponding document.

Databases: The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).

Register Transfer Language (RTL)

RTL (Register Transfer Language)

- Provides a language for describing the behavior of computers in terms of step-wise register contents
- Provides a formal means of describing machine structure and function
- Is at the "just right" level for machine descriptions
- Does not replace hardware description languages
- Can be used to describe *what* a machine does (an Abstract RTL) without describing *how* the machine does it
- Can also be used to describe a particular hardware implementation (A Concrete RTL)

A Note about Specification Languages

- They allow the description of *what* without having to specify *how*.
- They allow precise and unambiguous specifications, unlike natural language.
- Now the designer must debug the specification!
- Specifications can be automatically checked and processed by tools.
  - An RTL specification could be input to a simulator generator that would produce a simulator for the specified machine.
  - An RTL specification could be input to a compiler generator that would generate a compiler for the language, whose output could be run on the simulator.

Register Transfer Languages

- RTL describes the behavior of computers as stepwise transformations on register contents.
- Construct resembles FORTRAN, PASCAL, and C.
- Describe specific computers at the hardware level
- Variables correspond to the hardware registers
- Operations correspond to the hardware logic
- Verilog is becoming the standard design language in industry

RTL Construct #1: Declarations

- Defines one or more register entities
- Number of bits in each register
- Indexing convention for these bits
- The declarations are of the form declare register R1(S1:E1), R2 (S2:E2),R3 (S3:E3)
- R1,R2,RN denote the registers declares
- R[32] denotes an array of registers declared
- S1,S2,SN the starting index of the registers
- E1,E2,EN the ending index of the registers
- The number of bits in register R1 is E1-S1+1
- Note:The bit indexing convention throughout this course assigns index 0 to the least significant bit.

RTL Construct #1: Declarations

- Buses
- A special class of connection between registers
- B1 (S1:E1), B2 (S2:E2), etc

RTL Construct #2: Transfer Statements

- A set of input registers
- An output register
- Transformation writes output register based on the original contents of the input registers.
- Each transformation is performed in one clock cycle.
- Example transformations: AND, OR, XOR, ADD, SUBTRACT, SHIFT transformation vary significantly among different computers
- The register-transfer statements are of the form:

$$L: \ Z = F \ (X1, X2, \ldots XN)$$

- where X1,X2,XN denote the input registers
- Z the output register
- F the transformation
- L the label (name) of the statement
- label used by the control-transfer statements

RTL Construct #3: Control transfers

- Conditionally or unconditionally activates the execution of a statement.
- Without control-transfer, the computation executes sequentially till the end
- Control-transfer redirects this sequential execution by activating a nonsequential statement.
- Unconditional control-transfer are of the form

$$L1: goto \ L2$$

- where L1 is the label of the control transfer statement
- L2 is the label of the statement to be activated.

RTL Construct #3: Control transfers

- When an unconditional control-transfer statement is executed, the statement with label $L \text{ sub } 2$ is always activated.
- Conditional control-transfer of the form

    L1: if *(Condition1)* then goto $L \text{ sub } 2$
- where *Condition1* is a specified state of a register.
- For example, $R1 == 0$ is a condition which is fulfilled if the contents of register R1 is 0.
    - Similar for $R[1] == 0$
- Conditional control transfers only activates the statement with label
- L2 when the condition is fulfilled. Otherwise, the execution continues sequentially.

RTL Summary

- A register-transfer language program is a list of declarations, register transfer statements, and control transfer statements
- Each program describes the behavior of a computer
- Many different programs describe the same function
- Many different computers can be designed to perform the same function
- Straightforward to derive the hardware design from RTL
- Hardware design consideration often has impact on the derivation RTL programs
- Break down the operation into multiple operations each of which can be done in one cycle
- Multiple operations can be combined into one
- Deriving a register-transfer language program and designing hardware are steps of an iterative process